Abstract

A method for forming an antifuse interconnect structure, for a one-time fusible link, to be used with field-programmable gate arrays, has been developed. The process features the use of an amorphous silicon layer, used as the antifuse layer, with the sidewalls of the amorphous silicon layer protected by critical silicon nitride sidewall spacers, during the patterning/etch procedure of the overlying metal layer. The protective sidewall spacers prevent the amorphous Si antifuse from being etched by subsequent processes.